



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,585	10/10/2003	Masaki Takaoka	RHM-US020052	2584
22919 7590 05/14/2008 GLOBAL IP COUNSELORS, LLP 1233 20TH STREET, NW, SUITE 700 WASHINGTON, DC 20036-2680				
EXAMINER				
NADAV, ORI				
ART UNIT		PAPER NUMBER		
2811				
MAIL DATE		DELIVERY MODE		
05/14/2008		PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/605,585

Applicant(s)

TAKAOKA ET AL.

Examiner

Ori Nadav

Art Unit

2811

Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 April 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 14-22 is/are pending in the application.
- 4a) Of the above claim(s) 15, 17 and 22 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 14, 16 and 18-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SI/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Election/Restrictions

Claims 15, 17 and 22 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected embodiment, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 10/20/2004.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 16 and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claimed limitations of a third semiconductor element formed on a first surface of the another semiconductor substrate facing the semiconductor substrate having a gate electrode, a source electrode, and a drain electrode, as recited in claim 16, are unclear as to which element is facing the semiconductor substrate, and which element is having a gate electrode, a source electrode, and a drain electrode.

The claimed limitation of a third wiring, as recited in claim 21, is unclear as to whether this third wiring is the same element recited in dependent claim 14 or a different element.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 14 and 18-21, as best understood, are rejected under 35 U.S.C. 102(b) as being anticipated by Benecke et al. (5,049,460) or Akram et al. (6,107,109). Benecke et al. teach in figure (3I) and related text a semiconductor device, comprising:

a semiconductor substrate 1, 2 having a semiconductor substrate main unit and a thin portion, the thin portion being thinner than the semiconductor substrate main unit such that a recessed portion is formed in the semiconductor substrate at the thin portion, the thin portion having at least one through hole formed therein; and

a through wiring 7 including a first wiring formed on a first surface of the semiconductor substrate, a second wiring formed on a second surface opposite to the first surface, and a third wiring that fills the through hole, is formed along a wall surface of the recessed portion, and connects the first wiring and the second wiring,

wherein the first wiring has a first sub-wiring extending from the semiconductor substrate main unit to the thin portion on the first surface of the semiconductor substrate along a direction intersecting with a border of the semiconductor substrate main unit and the thin portion, and a second sub-wiring connected to the first sub-wiring and extending along the border on the thin portion, and

the through hole being formed at a location corresponding to a connection part of the first sub-wiring and the second sub-wiring, and

the through hole being formed at an end part of the second sub-wiring, and
a plurality of the through holes (see figure 1) formed under the second sub-wiring, and

a third wiring is formed on the wall surface of the recessed portion along a direction intersecting with the border.

Akram et al. teach in figure 1D and related text a semiconductor device, comprising:

a semiconductor substrate 10 having a semiconductor substrate main unit and a thin portion, the thin portion being thinner than the semiconductor substrate main unit such that a recessed portion is formed in the semiconductor substrate at the thin portion, the thin portion having at least one through hole formed therein; and

a through wiring including a first wiring 26 formed on a first surface of the semiconductor substrate, a second wiring 36, 38 formed on a second surface opposite to the first surface, and a third wiring 34 that fills the through hole, is formed along a wall surface of the recessed portion, and connects the first wiring and the second wiring,

wherein the first wiring has a first sub-wiring extending from the semiconductor substrate main unit to the thin portion on the first surface of the semiconductor substrate along a direction intersecting with a border of the semiconductor substrate main unit and the thin portion, and a second sub-wiring connected to the first sub-wiring and extending along the border on the thin portion, and

the through hole being formed at a location corresponding to a connection part of the first sub-wiring and the second sub-wiring, and

the through hole being formed at an end part of the second sub-wiring, and
a plurality of the through holes formed under the second sub-wiring, and
a third wiring is formed on the wall surface of the recessed portion along a direction intersecting with the border.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 16, as best understood, is rejected under 35 U.S.C. 103(a) as being unpatentable over (Benecke et al. or Akram et al.) in view of Applicant Admitted Prior Art (AAPA).

Benecke et al. and Akram et al. teach substantially the entire claimed structure, as applied to claim 14 above, except another semiconductor substrate disposed under the semiconductor substrate; and a third semiconductor element formed on a first surface of the another semiconductor substrate facing the semiconductor substrate having a gate electrode, a source electrode, and a drain electrode, wherein the through wiring of the

Art Unit: 2811

semiconductor substrate is connected to at least one of the source electrode and the drain electrode of the third semiconductor element.

AAPA teaches in figure 24 and paragraphs [0004] to [0007] another semiconductor substrate disposed under the semiconductor substrate; and a third semiconductor element formed on a first surface of the another semiconductor substrate facing the semiconductor substrate having a gate electrode, a source electrode, and a drain electrode, wherein the through wiring of the semiconductor substrate is connected to at least one of the source electrode and the drain electrode of the third semiconductor element.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to another semiconductor substrate disposed under the semiconductor substrate; and a third semiconductor element formed on a first surface of the another semiconductor substrate facing the semiconductor substrate having a gate electrode, a source electrode, and a drain electrode, wherein the through wiring of the semiconductor substrate is connected to at least one of the source electrode and the drain electrode of the third semiconductor element in Benecke et al. or Akram et al.'s device, in order to reduce the size of the semiconductor device.

Response to Arguments

Applicant's arguments with respect to claims 14, 16 and 18-21 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-4670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
5/14/2008

/ORI NADAV/
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800